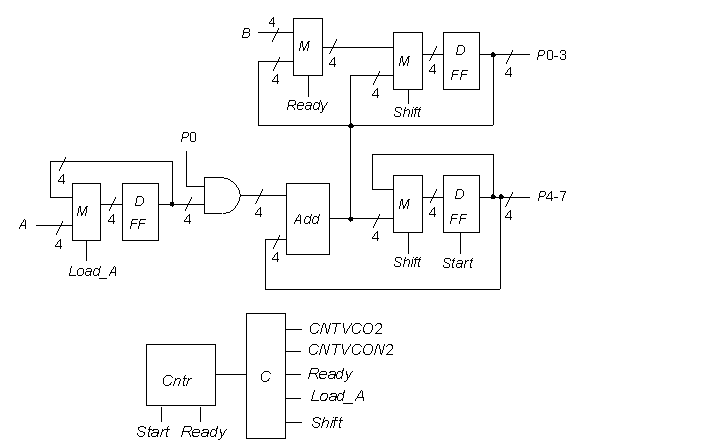
**ISCAS-89 s344/s349 4x4 Add-Shift Multiplier**



**Statistics:** 9 inputs; 11 outputs; 175/176 gates;

**Function:** The high-level functional model for the s344/s349 4-bit multiplier is shown above. It consists of 16 multiplexers, eight D-type flip-flops, four D-type flip-flops with reset, three T -type flip-flops, one 4-bit full adder, and one 4-bit AND. The circuit is controlled by a 3-bit counter, that when reset by the Start input, counts from 0 to 5. During a count of 0, the A input is loaded; between the counts 1-4, an add and shift procedure forms the multiplication product; and at a count of 5, the Ready line goes to 1, and holds the counter state fixed.

s344 and s349 have the same function, but have slightly different implementations.

**Models:**

* [s344 ISCAS-89 netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s344.isc)
* [s349 ISCAS-89 netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s349.isc)
* [s349 Verilog hierarchical structural model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s349.v)
* [s344/s349 Verilog hierarchical behavioral model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s344b.v)
* [s344/s349 complete gate-level tests](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s344.tests)